

Fig 1A

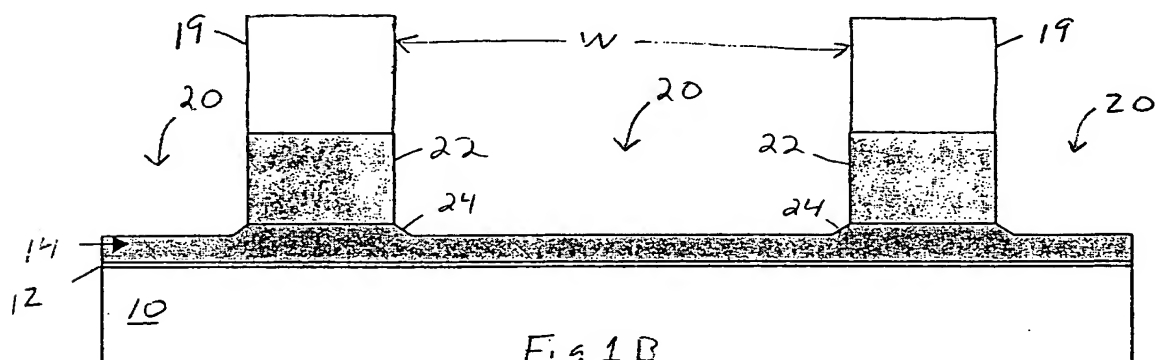


Fig 1B

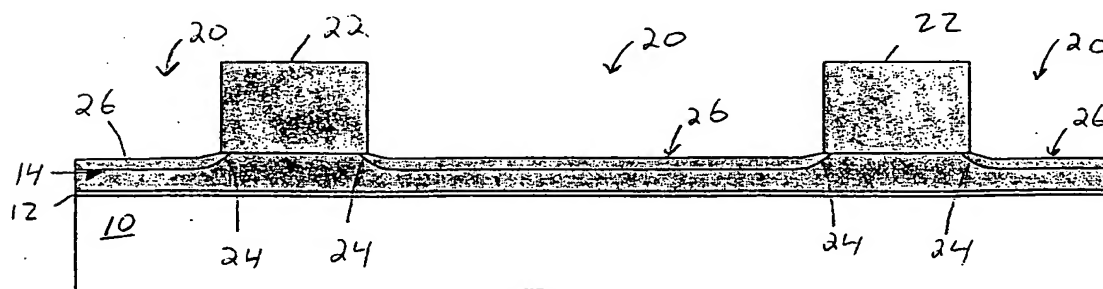


Fig 1C

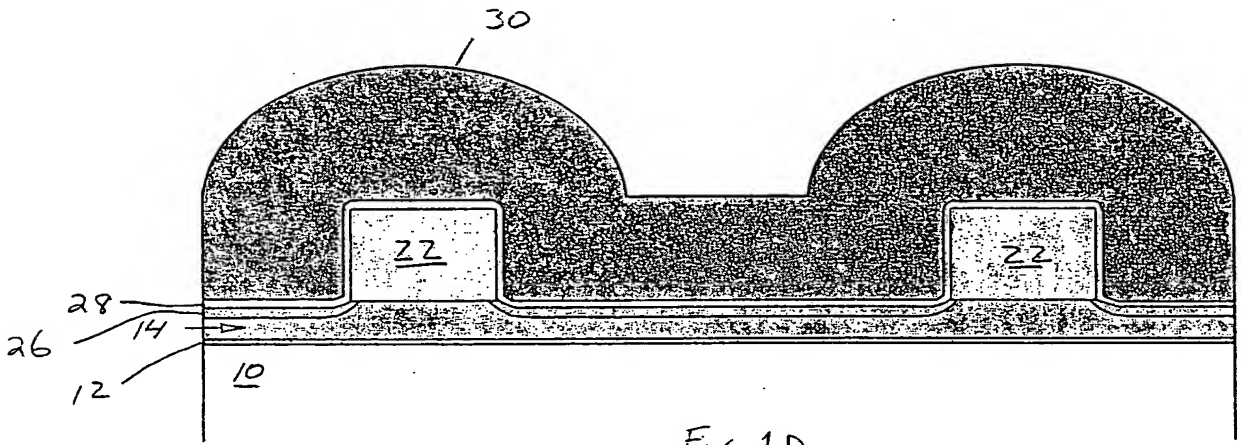


Fig 1D

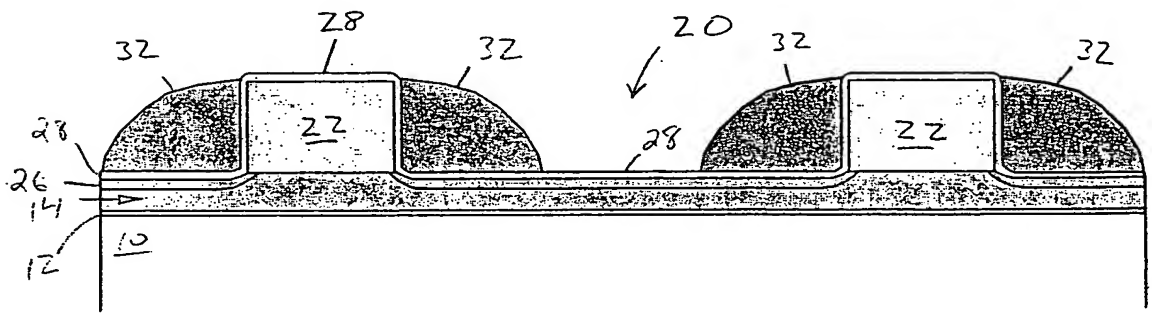
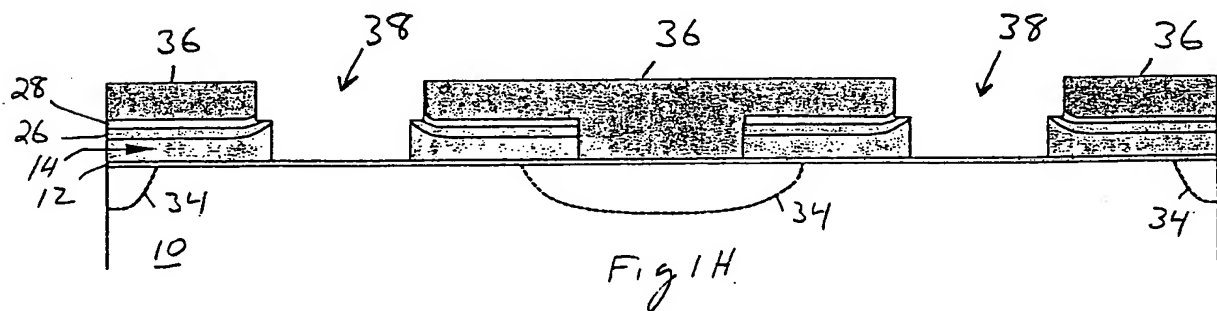
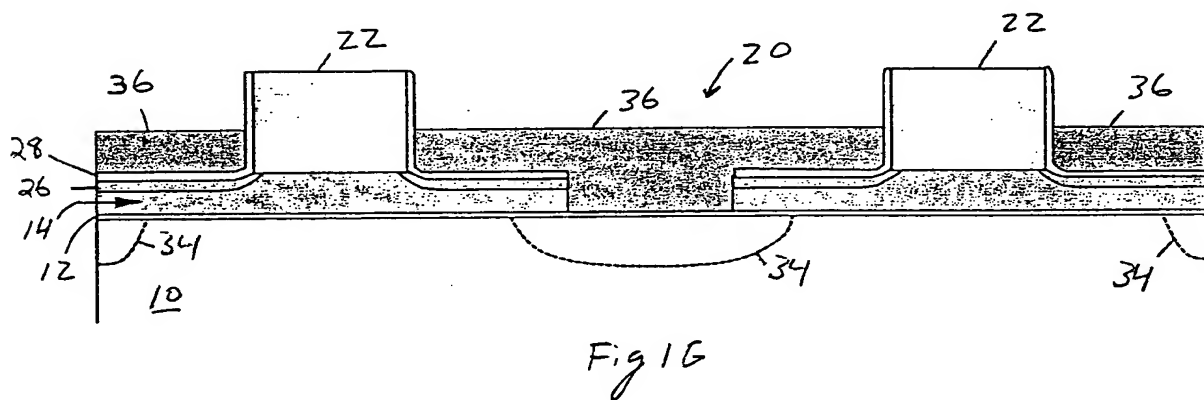
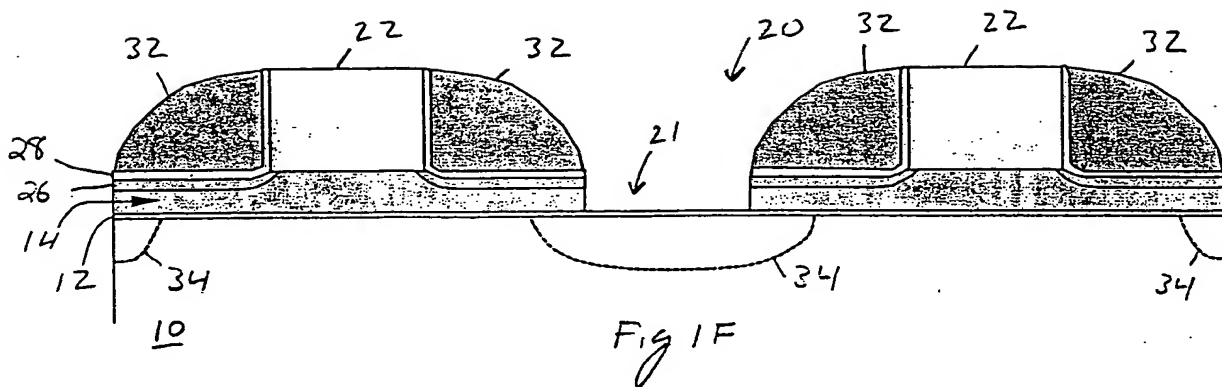
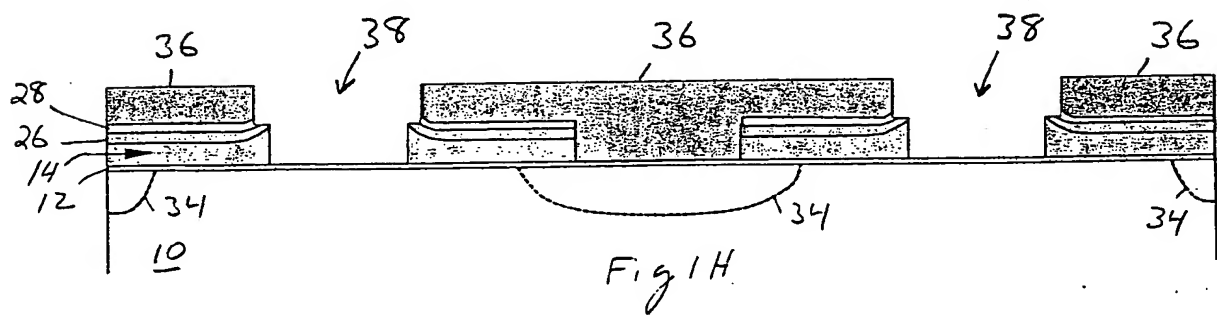
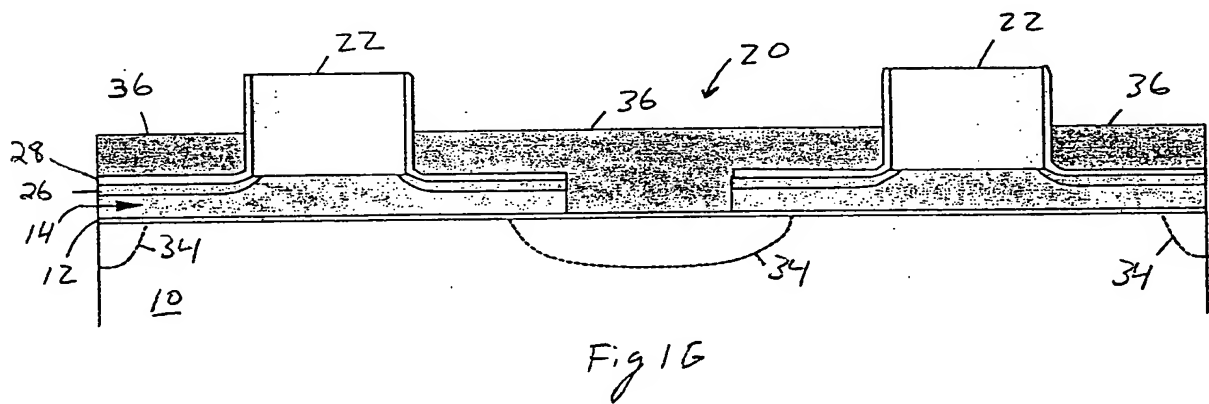
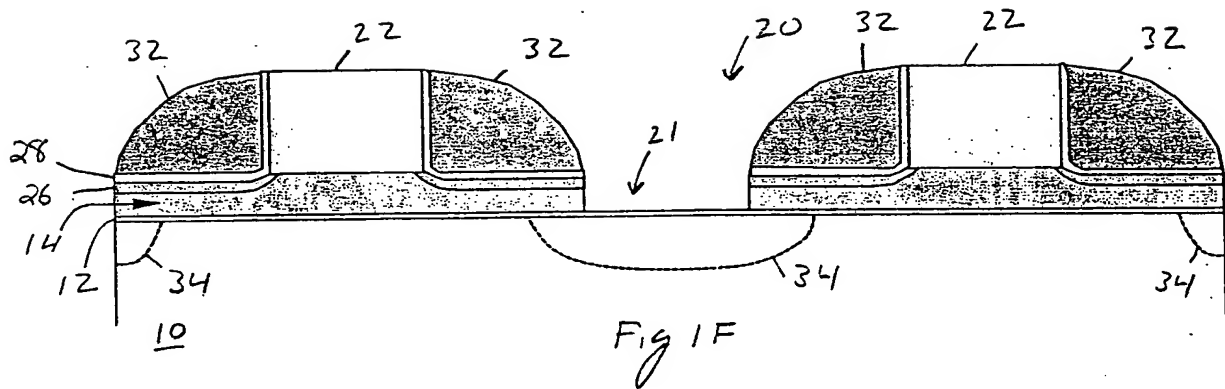
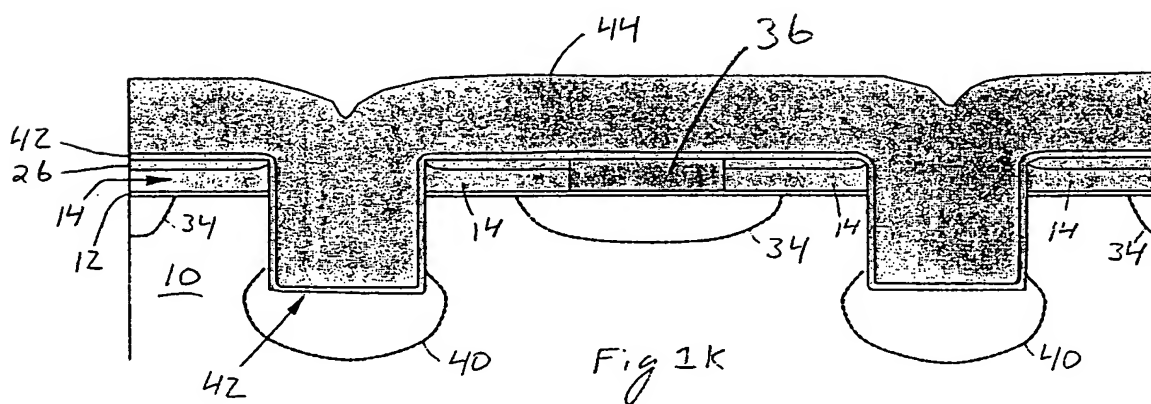
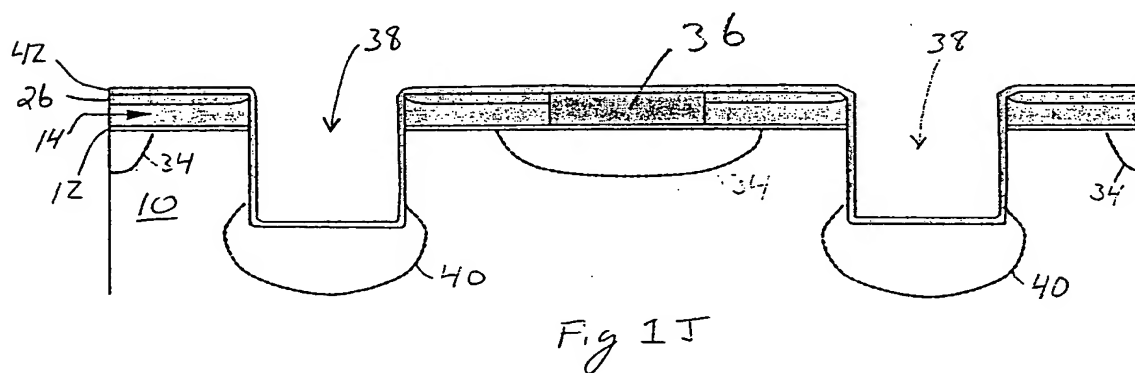
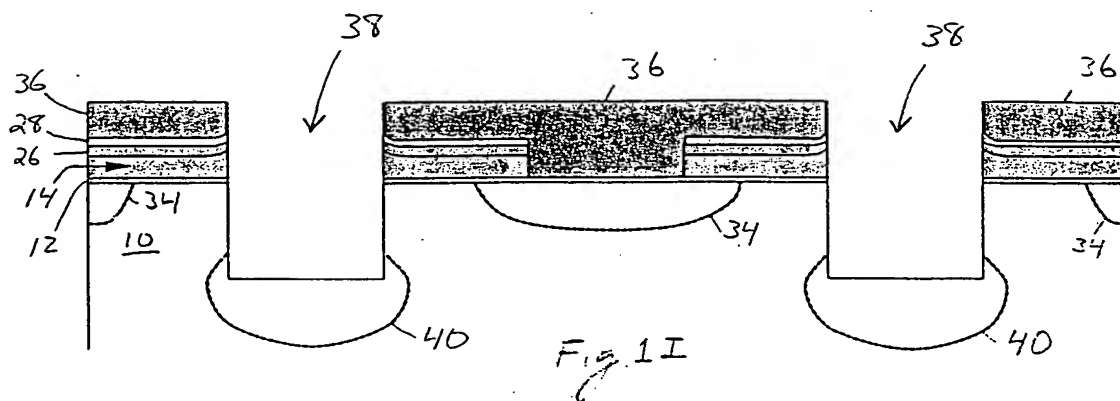


Fig 1E







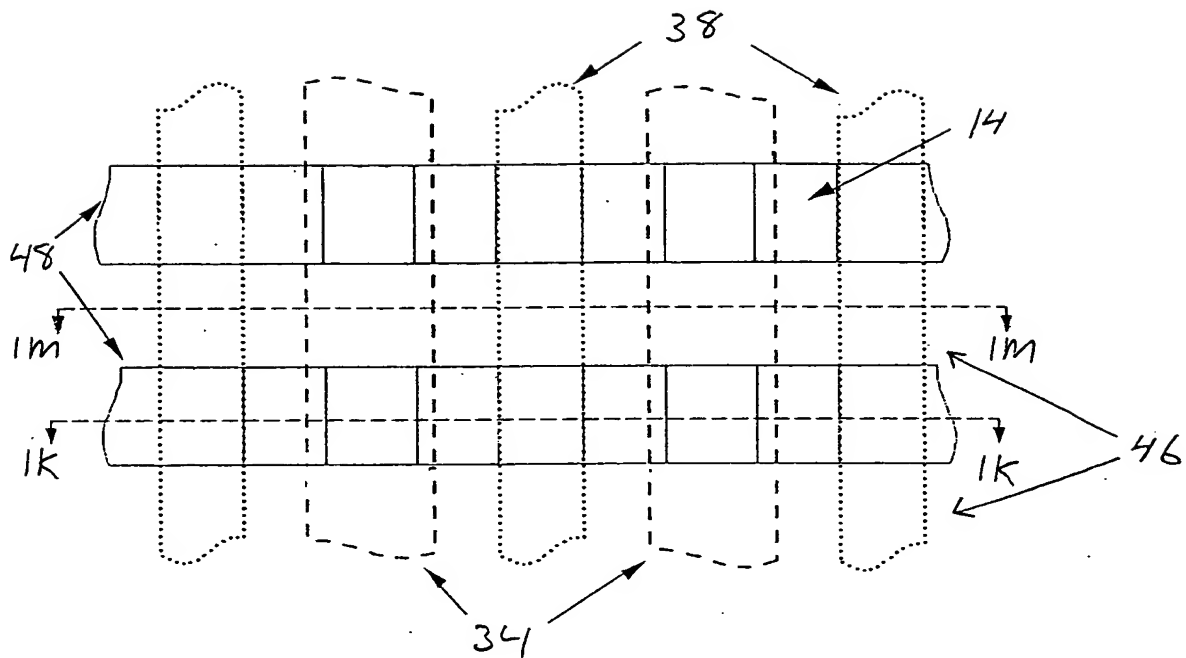


Fig 1L

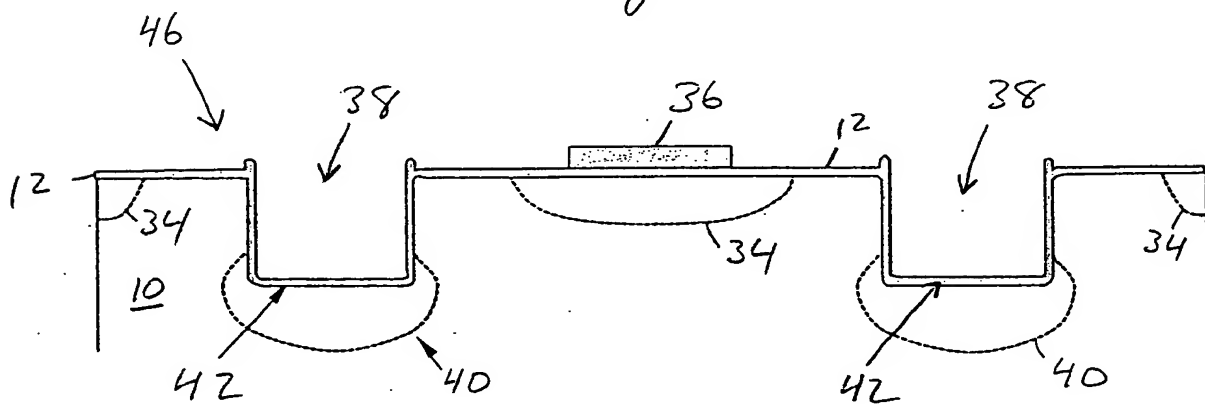
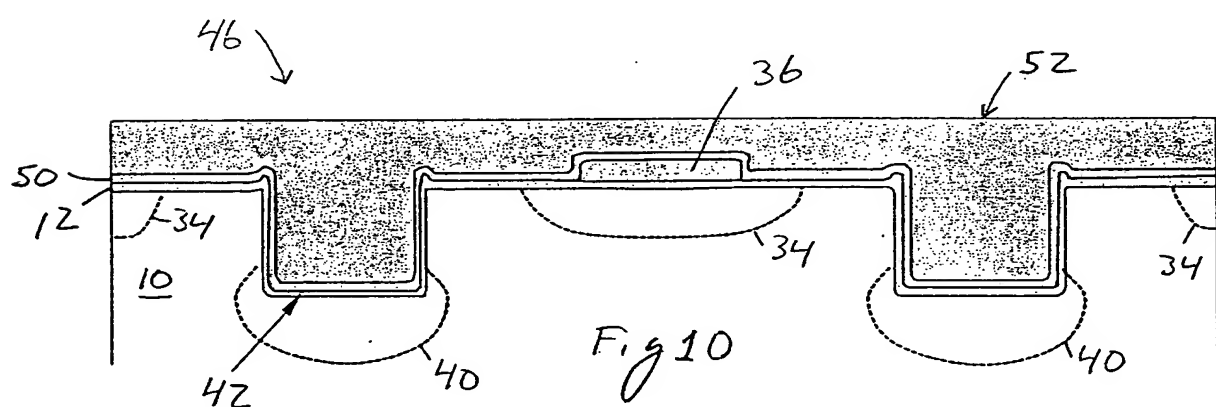
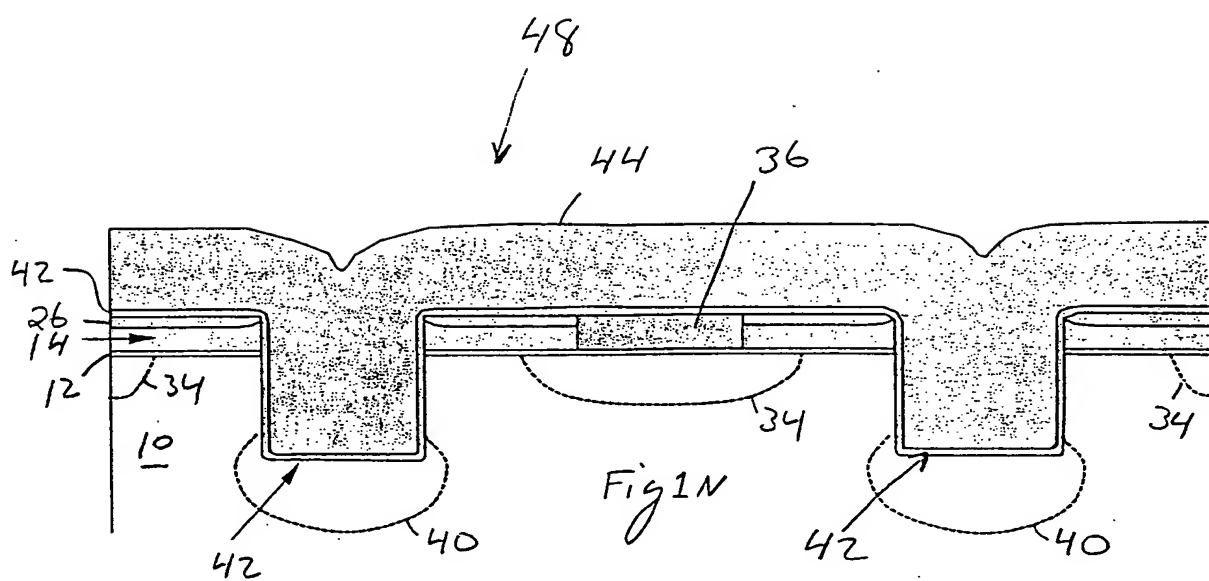


Fig 1m



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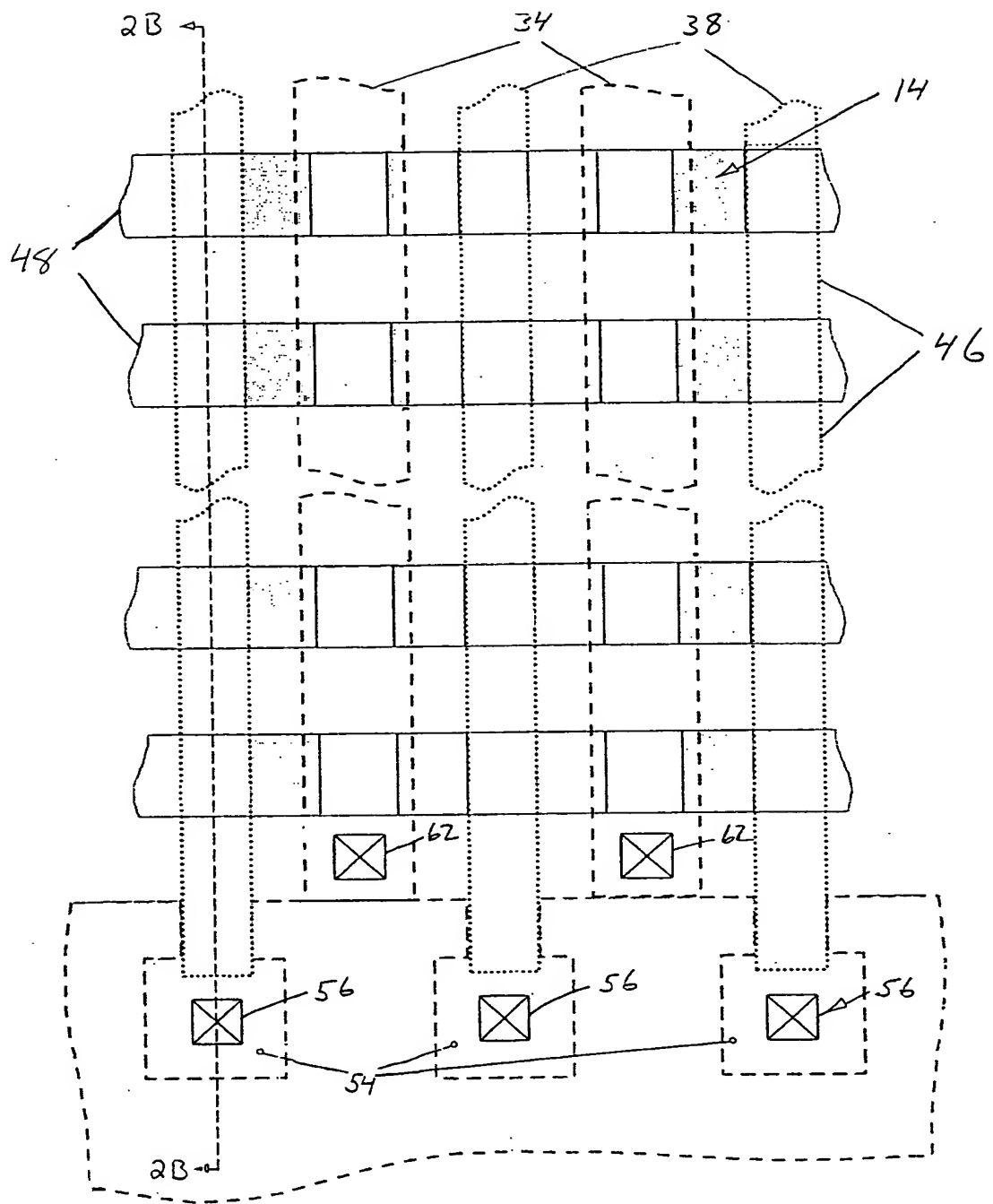


Fig 2A



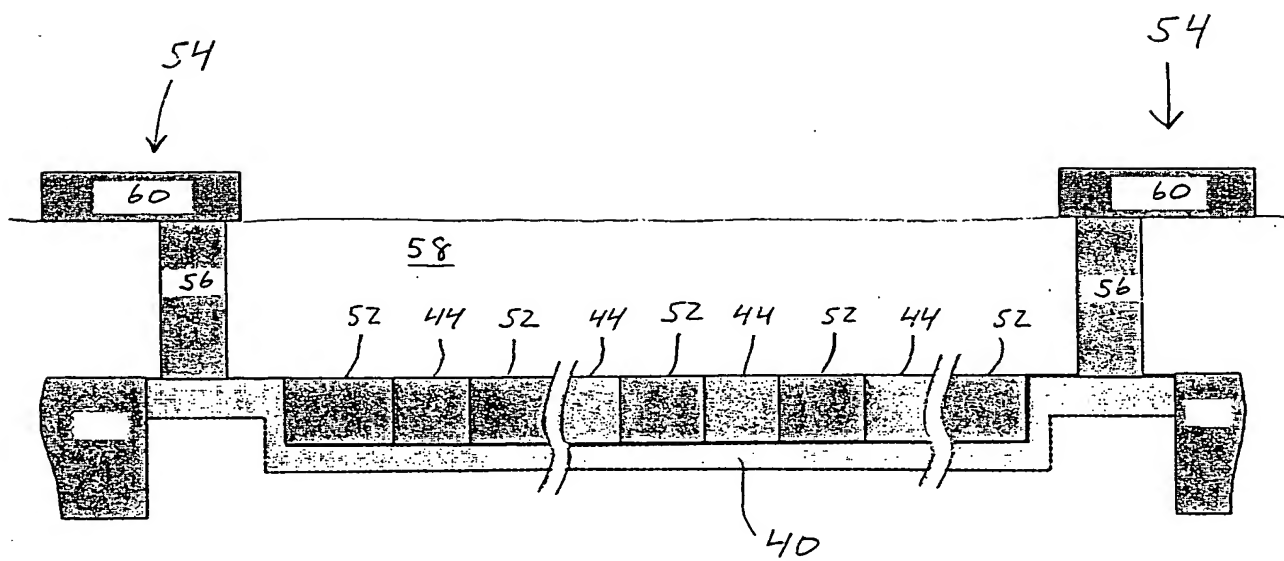


Fig 2B

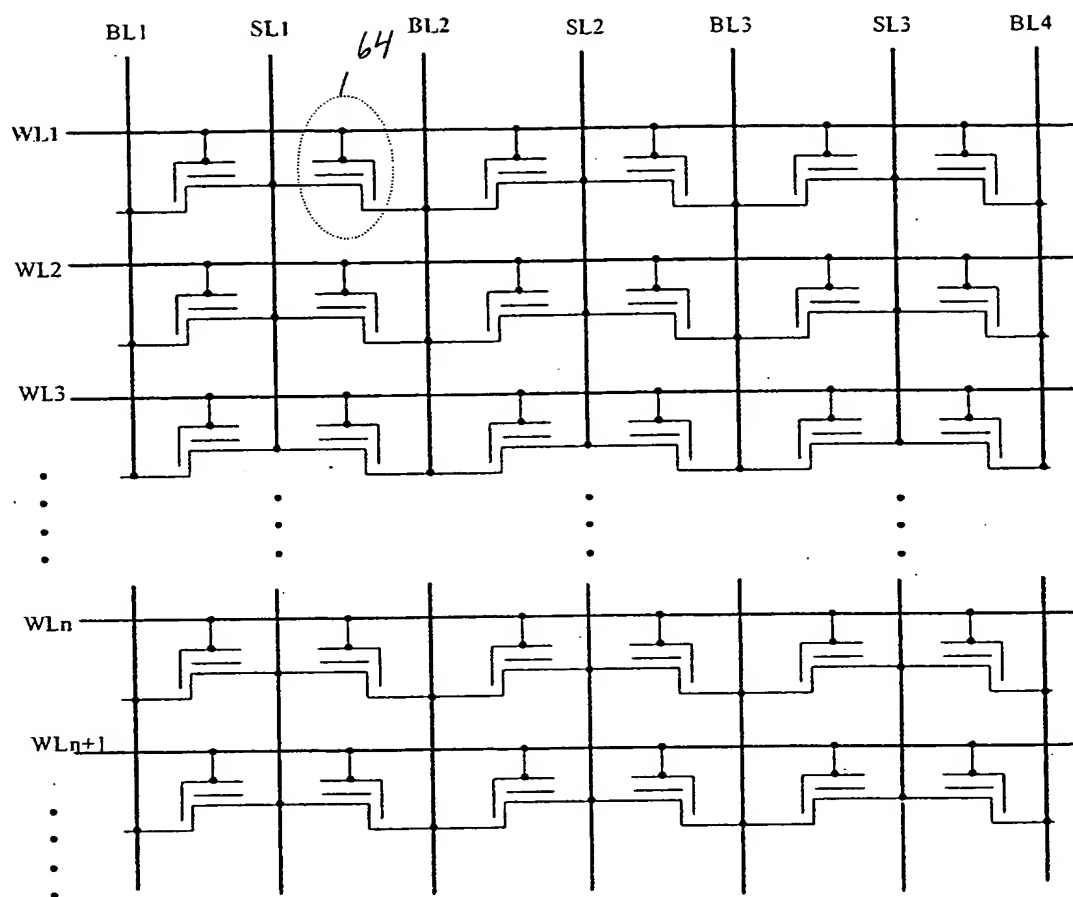
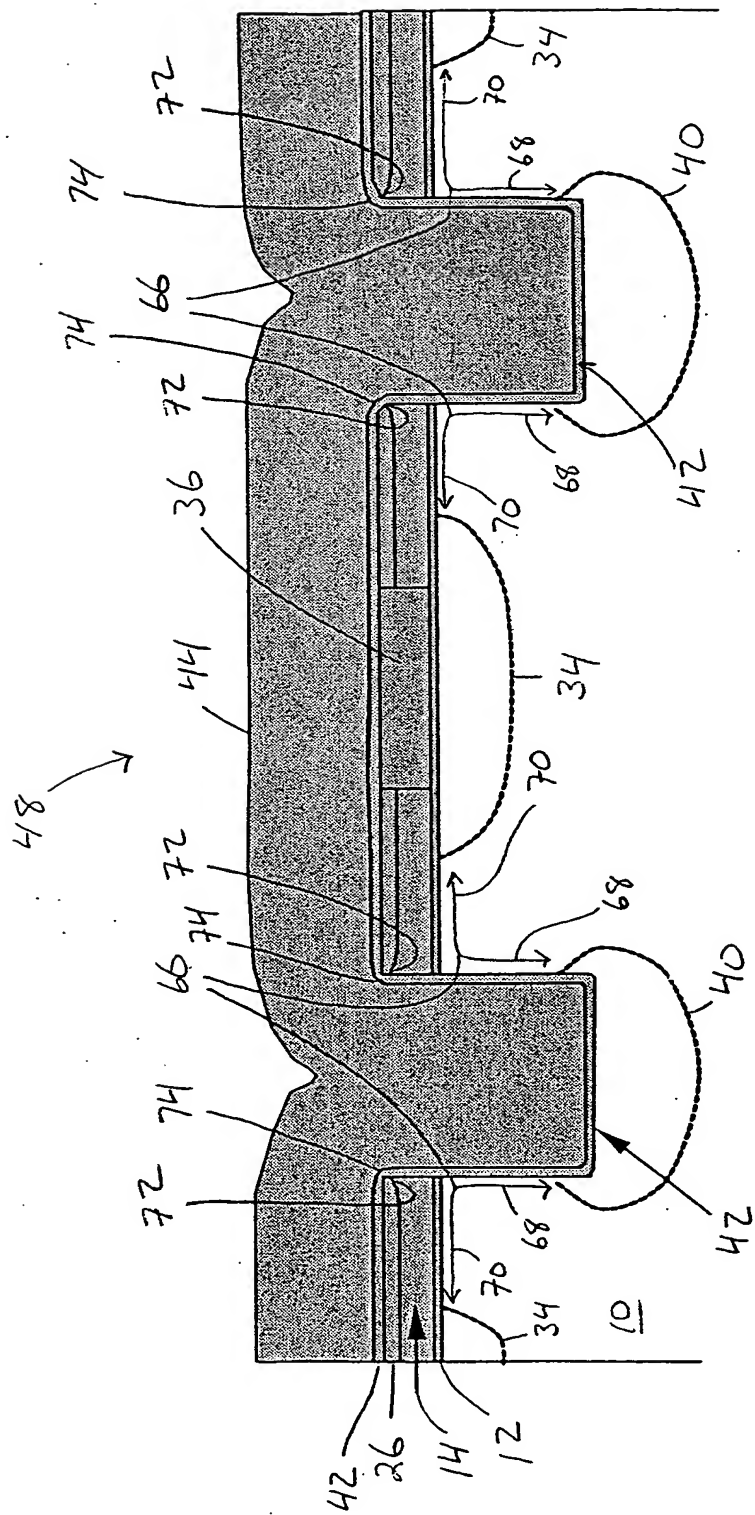
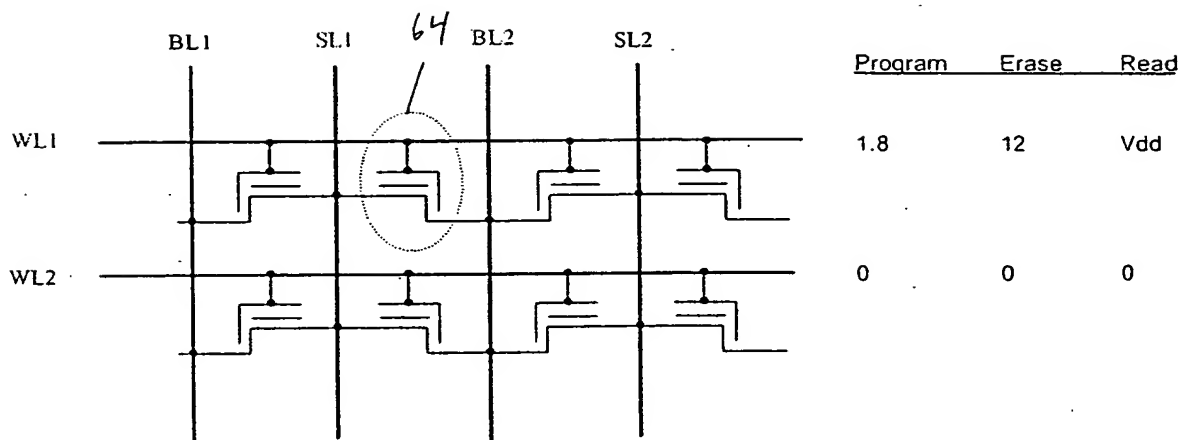


Fig 3





<u>Program</u>	Vdd (inhibit)	Vpp (e.g. 9-10V)	Vdp (0.5-1V)	0 (inhibit)
<u>Erase</u>	0	0	0	0
<u>Read</u>	0	0	-1V	0

Fig 5

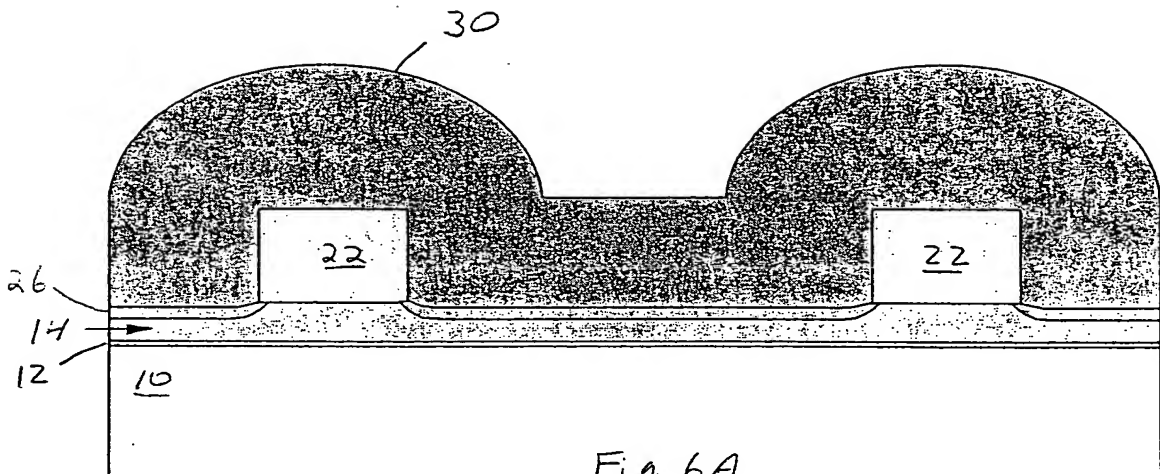


Fig 6A

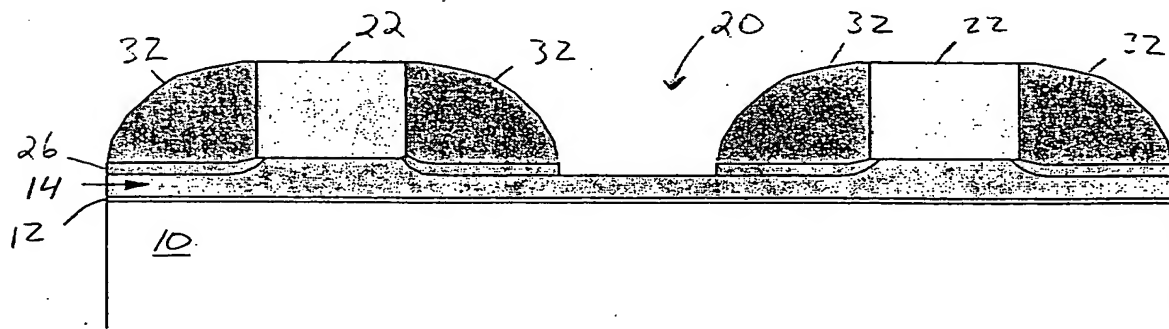
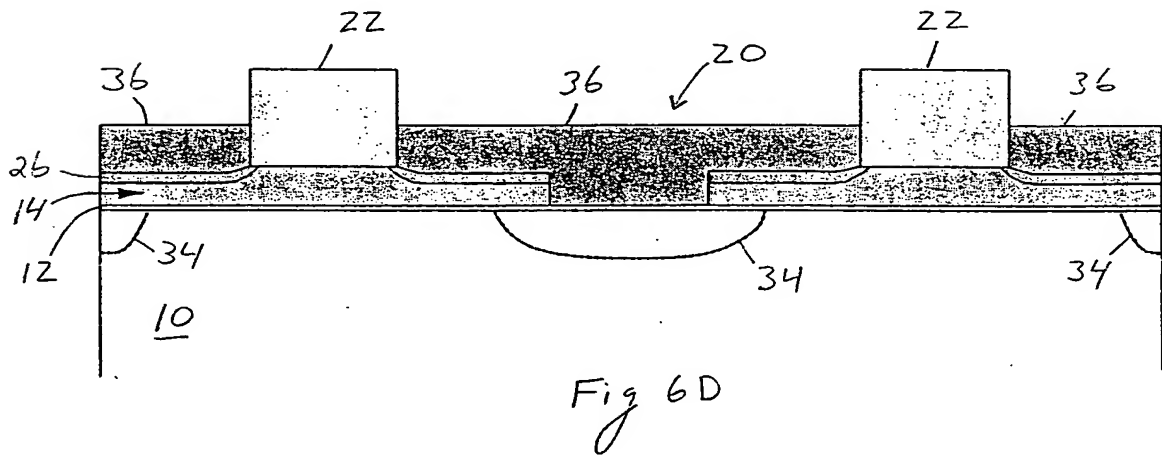
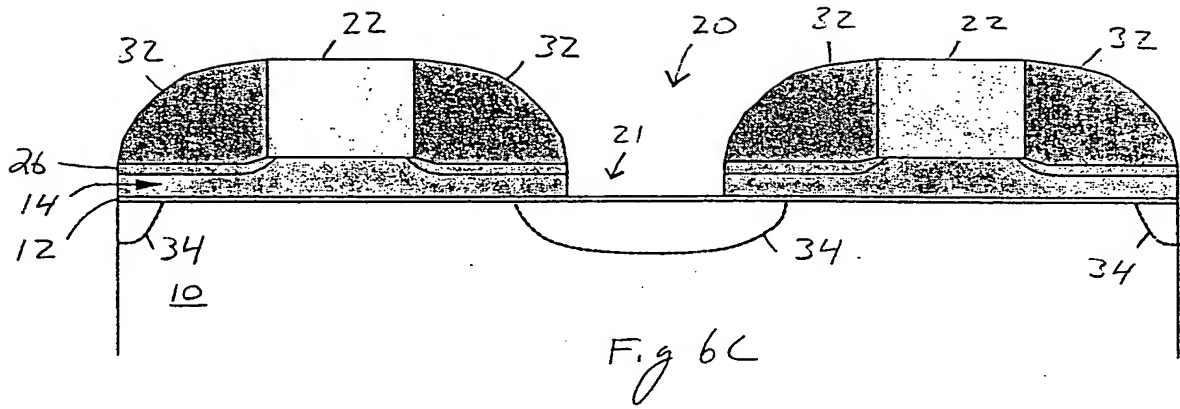


Fig 6B



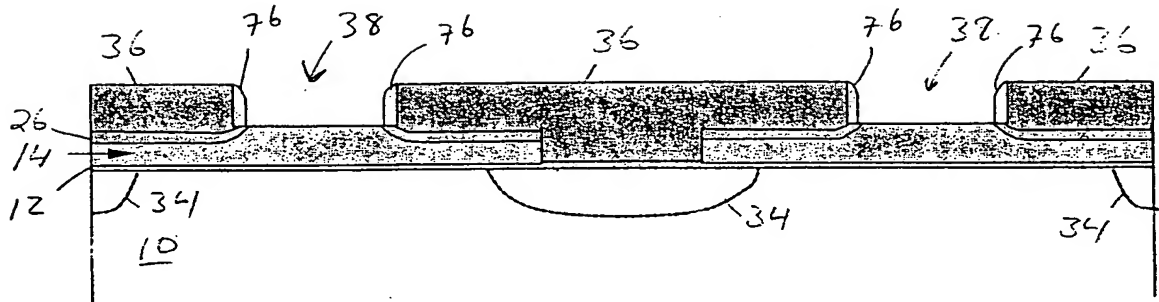


Fig 6 E

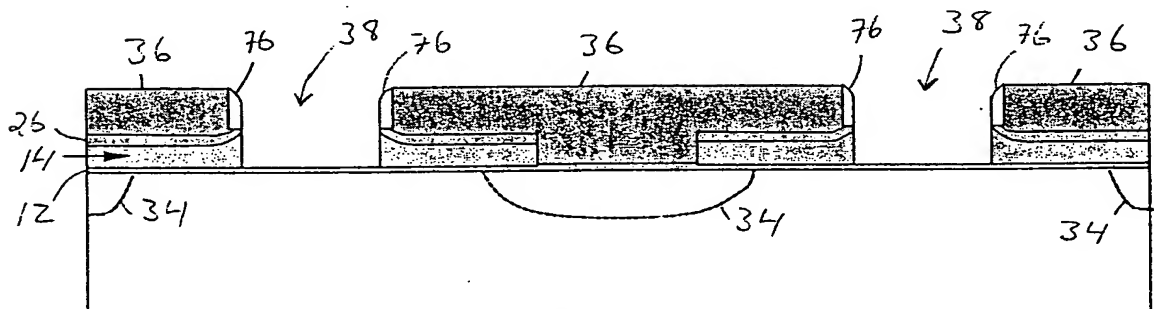


Fig 6 F

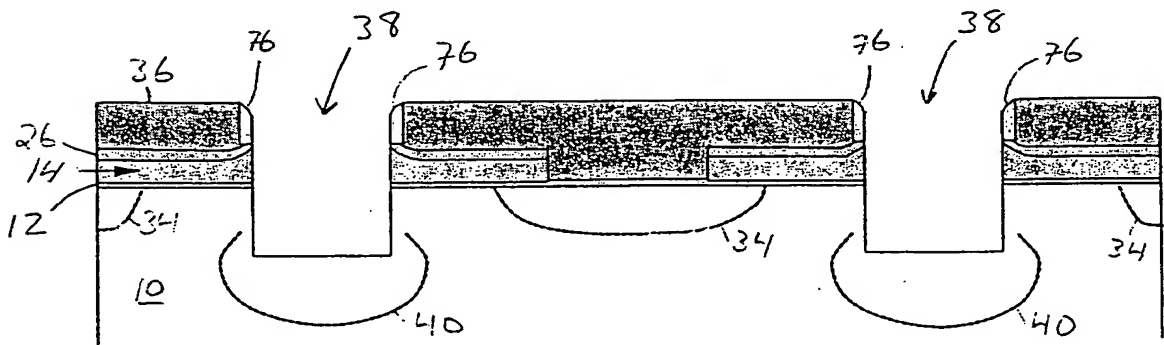


Fig 6 G

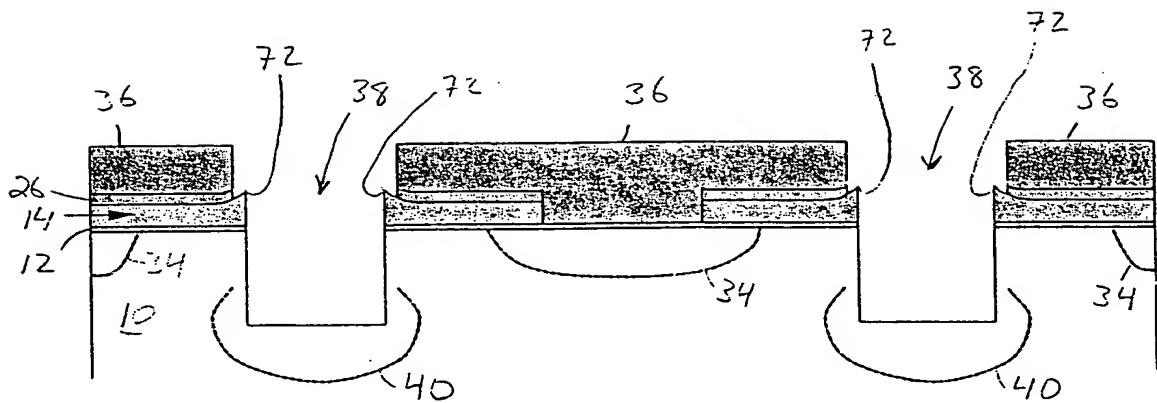


Fig 6H

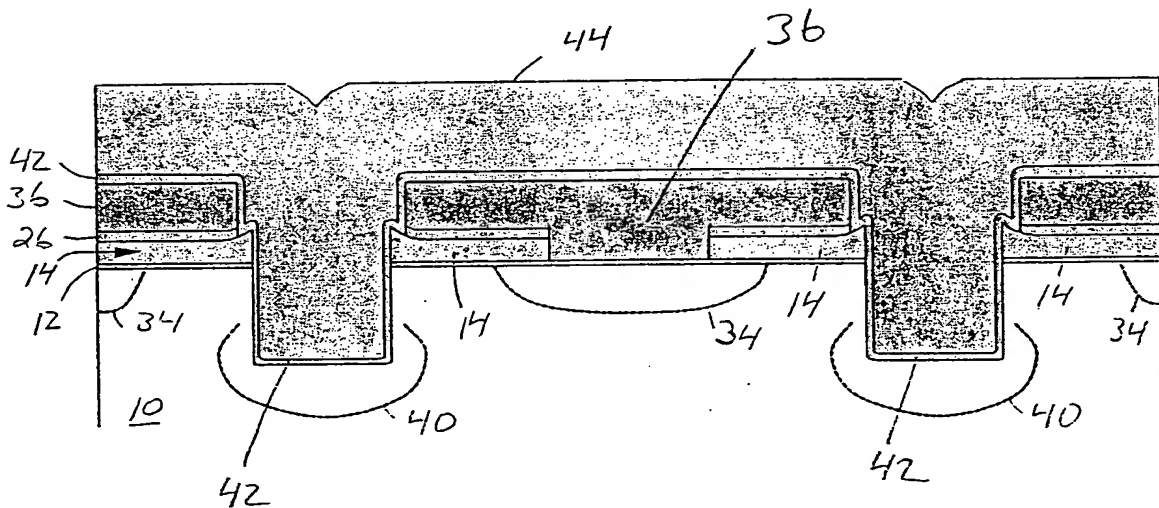


Fig 6 I



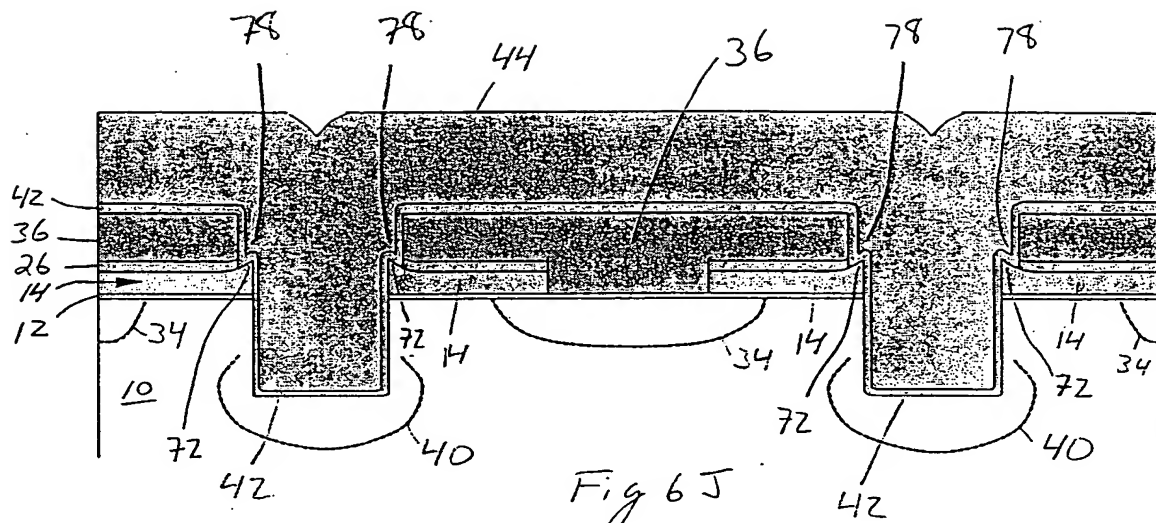


Fig 6 J

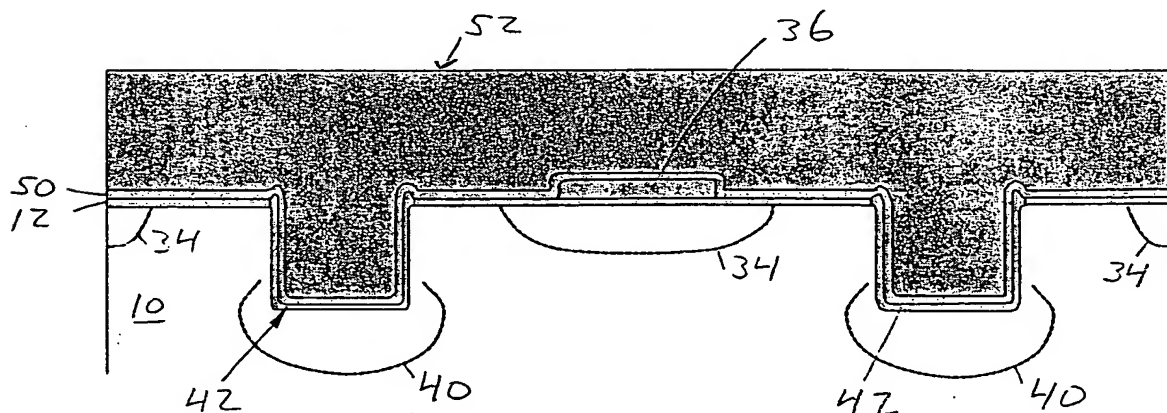


Fig 6 K

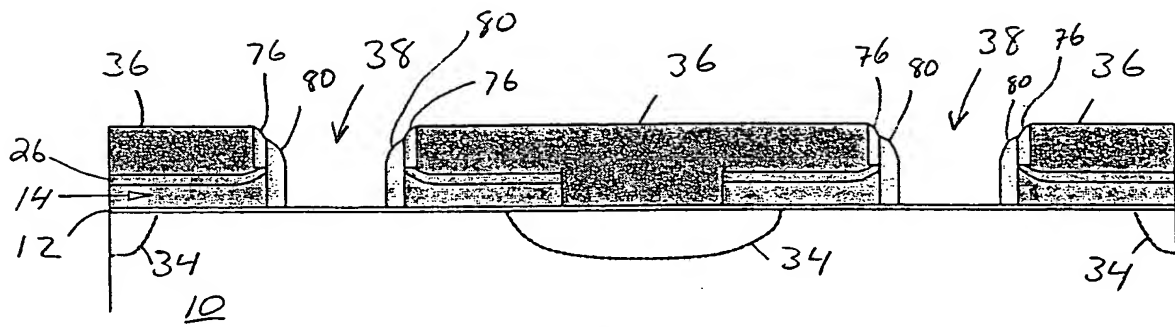


Fig 7A

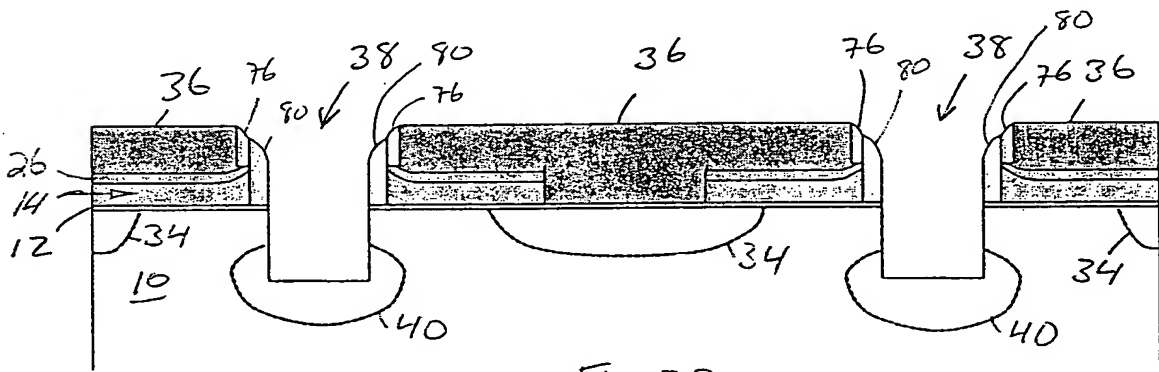


Fig 7B

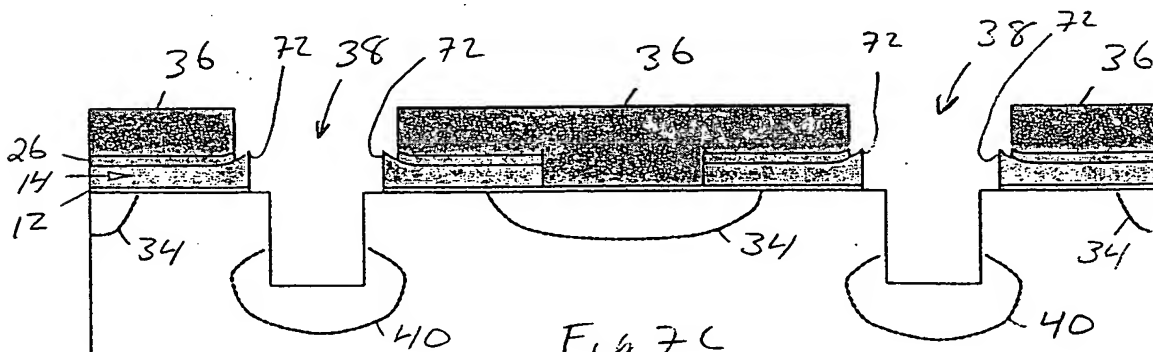


Fig 7C

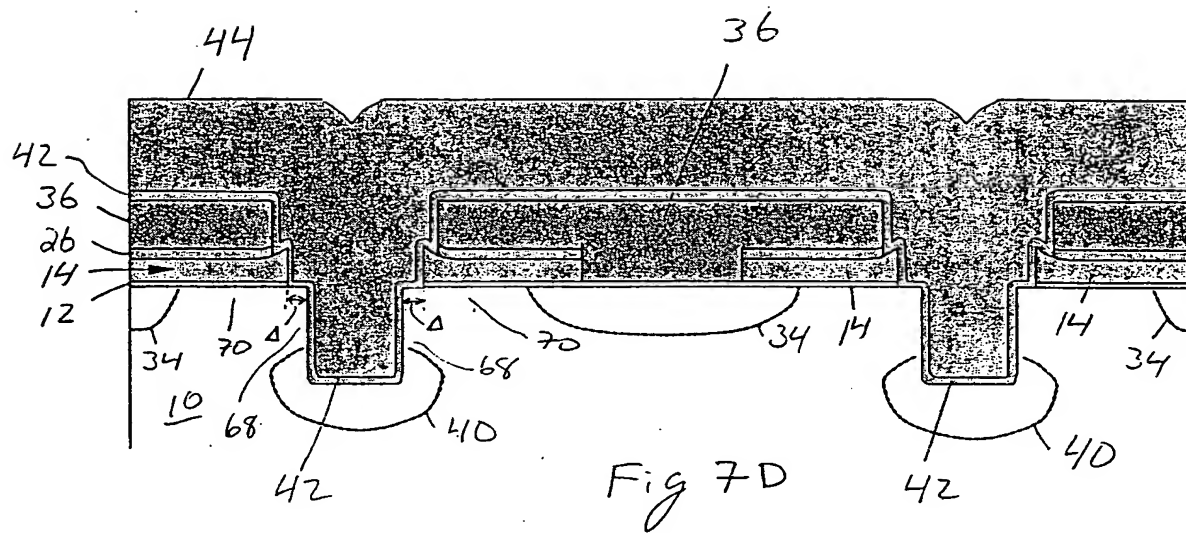


Fig 7D